IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex Parte Lines

Application for Patent: 10/667,152

Filed: September 16, 2003

Group Art Unit: 2183

Examiner: Aimee J. Lee

For:

ASYNCHRONOUS MULTIPLE-ORDER ISSUE SYSTEM ARCHITECTURE

AMENDED APPEAL BRIEF

Weaver Austin Villeneuve & Sampson LLP
P.O. Box 70250
Oakland, CA 94612-0250
Attorneys for Appellant

CERTIFICATE OF EFS-WEB TRANSMISSION
I hereby certify that this correspondence is being transmitted electronically through EFS-WEB to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450 on November 5, 2008.

Signed: /Emma Durrell/
Name: Emma Durrell

TABLE OF CONTENTS

1. REAL PARTY IN INTEREST

[37 CFR 41.37(c)(1)(i)]

The real party in interest is Fulcrum Microsystems, Inc., of Calabasas, California.

2. RELATED APPEALS AND INTERFERENCES

[37 CFR 41.37(c)(1)(ii)]

A Pre-Appeal Brief Request for Review was filed on June 3, 2008, along with the Notice of Appeal which precipitated the present appeal. A Pre-Appeal Brief conference was held. A copy of the Notice of Panel Decision from Pre-Appeal Brief Review dated July 16, 2008, is included herewith in the Related Proceedings Appendix.

The undersigned is not aware of any other related appeals or interferences.

3. STATUS OF CLAIMS

[37 CFR 41.37(c)(1)(iii)]

The following claims have been rejected and appealed: 1-22, 27-44, and 49.

The following claims have been cancelled: 23-26 and 45-48.

The claims on appeal are reproduced below in the Appendix at Section 9 of this Appeal Brief.

4. STATUS OF AMENDMENTS

[37 CFR 41.37(c)(1)(iv)]

Amendments filed with Applicants' Request for Continued Examination filed August 2, 2007, have been entered. No amendments were filed in response to the Office Action dated October 17, 2007, or the Final Rejection dated May 13, 2008.

5. SUMMARY OF CLAIMED SUBJECT MATTER

[37 CFR 41.37(c)(1)(v)]

The claimed invention relates generally to "an asynchronous multiple-issue architecture in which the issue of instructions in N parallel instruction pipelines are staggered in time…such that N instructions are issued each cycle, but, due to the alternating (and therefore sequential) issuance, the interdependency between closely spaced instructions do not require the complexities or suffer from the resulting underperformance encountered in the typical multiple-issue synchronous system." Page 6, paragraph [0022].

5.1. *Independent Claim 1*

Claim 1 recites "[a]n asynchronous circuit for processing units of data having a program order associated therewith." See, for example, [0005], [0007], [0022], [0024], [0027], [0045], and [0046]. The asynchronous circuit is "configured to employ asynchronous flow control to facilitate transmission of the data units." See, for example, [0017] and [0023]. The asynchronous flow control is "characterized by an average cycle time." See, for example, [0022] and [0023]. The circuit includes "an N-way-issue resource comprising N parallel pipelines" each of which is "operable to transmit a subset of the units of data in a first-in-first-out manner." See, for example, [0005], [0022], and [0045]. The data units "are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time." See, for example, [0022] and [0023]. The asynchronous circuit "is operable to sequentially control transmission of the units of data in the pipelines such that the program order is maintained." See, for example, [0005], [0007], [0022], [0024], [0027], [0045], and [0046].

5.2. *Independent Claim 22*

Claim 22 is similar in scope to claim 1 and recites "[a]t least one computer-readable medium having data structures stored therein representative of" such an asynchronous circuit. In addition to the support recited above for the corresponding limitations in claim 1, see, for example, [0050].

5.3. *Independent Claim 27*

Claim 27 is similar in scope to claim 1 and recites "[a] set of semiconductor processing masks representative of" such an asynchronous circuit. In addition to the support recited above for the corresponding limitations in claim 1, see, for example, [0050].

5.4. *Independent claim 28*

Claim 28 recites "[a] heterogeneous system for processing units of data having a program order associated therewith, the system comprising an N-way issue resource and at least one multiple-issue resource having an order different from N." See, for example, [0005], [0006], [0028], and [0044]. The N-way issue resource is "configured to employ asynchronous flow control to facilitate transmission of the data units." See, for example, [0017] and [0023]. The asynchronous flow control is "characterized by an average cycle time." See, for example, [0022] and [0023]. The N-way issue resource is "configured such that the units of data are issued to N parallel pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time." See, for example, [0022] and [0023]. The system further includes "interface circuitry operable to facilitate communication between the N-way-issue resource and the at least one multiple-issue resource and to preserve the program order in all of the resources." See, for example, [0005], [0007], [0022], [0024], [0027], [0037], [0042], [0045], and [0046].

5.5. *Independent claim 44*

Claim 44 is similar in scope to claim 28 and recites "At least one computer-readable medium having data structures stored therein representative of" such a heterogeneous system. In addition to the support recited above for the corresponding limitations in claim 28, see, for example, [0050].

5.6. *Independent claim 49*

Claim 49 is similar in scope to claim 28 and recites "[a] set of semiconductor processing masks representative of" such a heterogeneous system. In addition to the support recited above for the corresponding limitations in claim 28, see, for example, [0050].

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

[37 CFR 41.37(c)(1)(vi)]

The issue which Appellant believes to be most pertinent to the present appeal:

The Examiner has failed to establish a prima facie case of unpatentability because the Examiner has ignored important limitations in the claims which are neither shown nor suggested by the art of record.

In addition, the combination of the Vegesna and Chu references as proposed by the Examiner results is unsupportable for multiple reasons.

The specific ground of rejection to be reviewed is as follows:

Ground I: Whether any of claims 1-22, 27-44, and 49 are unpatentable under 35 U.S.C. 103(a) over U.S. Patent No. 5,488,729 (Vegesna) in view of U.S. Patent No. 5,920,899 (Chu); or the combination of Vegesna and Chu in view of any of U.S. Patent No. 5,428,811 (Hinton), *SiGe Come of Age in the Semiconductor Industry* by Ahlgren et al. (Ahlgren), or U.S. Patent No. 5,832,303 (Murase).

7. ARGUMENT

[37 CFR 41.37(c)(1)(vii)]

7.1. Ground I

Claim 1 is representative of the group of claims rejected over the combination of Vegesna and Chu, as well as the combinations of Vegesna and Chu with Hinton, Ahlgren, and Murase, respectively. Therefore, the following argument focuses on the patentability of claim 1 over this combination. However, it will be understood with reference to these arguments that claims 2-22, 27-44, and 49 are patentable over this combination for at least the reasons discussed. The claims in this group therefore stand or fall together.

As described in the Background of the Invention of present application, synchronous processor architectures which issue multiple instructions each clock cycle "require complex schemes for determining, for example, whether two instructions may be executed at the same time. These complex schemes not only hamper system performance, but make multiple issue architectures difficult to verify." See paragraph [0003]. As set forth in previous responses, Vegesna is such a synchronous processor architecture, and provides such a complex verification scheme.

And as described in paragraph [0022] of the present application, "[t]he present invention provides an asynchronous multiple-issue architecture in which the issue of instructions in N parallel instruction pipelines are staggered in time...such that N instructions are issued each cycle, but, due to the alternating (and therefore sequential) issuance, the interdependency between closely spaced instructions do not

require the complexities or suffer from the resulting underperformance encountered in the typical multiple-issue synchronous system." That is, the present invention addresses the shortcomings systems like Vegesna's. As will be described below, none of the art of record teach or suggest such an approach.

As described in previous responses, a key aspect of the approach described in Vegesna is that instructions are issued to its parallel pipelines simultaneously. See, for example, column 1, lines 16-22; column 2, lines 56-61 and 64-67; column 3, lines 11-13; column 14, lines 59-61; column 23, lines 8-11; column 29, lines 34-37; etc. In fact, because Vegesna's architecture is controlled by a clock signal, units of data can only be issued to its pipelines on a clock transition, and can therefore only be issued to the pipelines simultaneously. See for example, the various figures relating units of data to clock cycles. And because the synchronous parallel pipelines process parallel data units simultaneously, elaborate measures are required to determine whether there are any dependencies between the data units and, if any are found, manipulate the flow of one or both pipelines to handle the dependency. As is well known, this is extremely expensive in chip resources and severely limits the scale and efficiency of N-way synchronous pipelines.

Chu, on the other hand, describes an "asynchronous pipeline that is divided into separate data and signal chains by moving the data register load signal buffer outside of the closed loop that generates the output request event from the input request event." This causes "the output request event to occur before output data is available." See Abstract. Significantly, and as is clear throughout the specification and drawings, Chu only describes the design and operation of a single pipeline (see, for example, FIGs. 7 and 15-17), and provides no teachings or suggestions as to how to implement multiple instances of his pipeline in parallel.

As will be discussed below, the combination of Vegesna and Chu is unsupportable. However, assuming for the sake of argument that one could successfully combine the teachings of Vegesna and Chu, the fact remains that important limitations recited in the claims of the present application are still neither taught nor suggested by the combination. That is, claim 1 of the present application explicitly recites that "data units are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time." This limitation is neither taught nor suggested by the cited references either alone, or in combination with each other.

First, as discussed above, Vegesna's approach *requires* that instructions be issued simultaneously. Thus, to suggest that such a teaching comes from Vegesna is simply incorrect.

Second, as discussed above, Chu describe only the implementation of single pipeline. Therefore, there can be no staggering of the issuing of data units "such that up to N data units enter the N pipelines during the average cycle time." That is, with only one pipeline, Chu can only issue one instruction per cycle by definition.

The Examiner points to columns 3-5 and various unrelated figures in Chu to support the assertion that this limitation is shown. However, as discussed above, Chu *cannot* show this limitation in that Chu only describes the design and operation of a single asynchronous pipeline. The passages to which the Examiner refers merely describe the passage of data between *serially* arranged stages in a *single* pipeline. This is clearly irrelevant to the claim limitation to which the Examiner is referring.

At most, the combination of Vegesna and Chu suggests the idea that one could implement multiple parallel asynchronous pipelines. However, the claims of the present application are not trying to capture such a generic notion. And there is absolutely no teaching or suggestion in either of the references as to how such a system might be accomplished. There is certainly nothing to teach or suggest a circuit in which "data units are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time."

Moreover, given the nature and purpose of the respective references, one of ordinary skill in the art would never be motivated to combine the teachings of Vegesna and Chu as proposed by the Examiner.

First, replacing each of the synchronous pipelines of Vegesna with an instance of the asynchronous pipeline of Chu would require some form of translation circuitry between synchronous domain embodied by the context in which Vegesna's pipelines are implemented, and the asynchronous domain embodied by each instance of Chu's pipeline. No such translation circuitry is taught or suggested.

Second, virtually all of the circuits designed for use with Vegesna's pipelines would need to be either significantly altered or completely replaced to make them compatible with the manner in which Chu's pipeline operates. For example, Vegesna's Intrapacket Scheduling Logic 76 and Interpacket Scheduling Logic 78

detect data dependencies within and between packets are both designed to operate in the synchronous domain and on the assumption that the pipelines with which they are interacting are synchronous pipelines to which data are simultaneously issued. The replacement of Vegesna's synchronous pipelines with instances of Chu's asynchronous pipeline would therefore necessitate a complete redesign of each of these circuits as they would not be operable with Chu's pipeline. These are merely two examples of the many circuits in Vegesna for which this is the case.

Finally, and most importantly, the Examiner's proposed combination of Vegesna and Chu completely ignores the problem being solved by Vegesna and the manner in which it is solved. As discussed, Vegesna makes it clear that the solution being proposed to the problem of issuing multiple instructions per clock cycle requires the simultaneous issuance of instructions to its pipelines. This feature of Vegesna's solution is stressed as critical because it is necessitated by the constraints of the context in which the solution is implemented, i.e., a synchronous domain controlled by a clock signal. It therefore strains credibility for the Examiner to suggest that one of skill in the art would attempt to incorporate an asynchronous pipeline in this context as this would not only ignore the main thrust of Vegesna's approach, but would introduce an entirely new set of technical problems for which neither of the references provides any guidance. Thus, the teaching of the references are incompatible.

In view of the fact that neither Vegesna nor Chu teaches or suggests an important limitation of claim 1, and because the teachings of the references are not combinable in the manner suggested by the Examiner, all of the rejections should be withdrawn.

8. CONCLUSION

In view of the foregoing, it is respectfully submitted that the Examiner's rejections of the claims of the present application as being unpatentable over the combination of Vegesna and Chu, or these references in combination with any of Hinton, Ahlgren, and Murase is erroneous. Accordingly, the rejection of claims 1-22, 27-44, and 49 under 35 U.S.C. §103(a) should be reversed.

Respectfully submitted,
Weaver Villeneuve Austin & Sampson LLP

/Joseph M. Villeneuve/

Joseph M. Villeneuve
Registration No. 37,460

Weaver Villeneuve Austin & Sampson LLP
Attorneys for Appellant

9. CLAIMS APPENDIX

[37 CFR 41.37(c)(1)(viii)]

CLAIMS ON APPEAL

1. (Previously presented) An asynchronous circuit for processing units of data having a program order associated therewith, the asynchronous circuit being configured to employ asynchronous flow control to facilitate transmission of the data units, the asynchronous flow control being characterized by an average cycle time, the circuit comprising an N-way-issue resource comprising N parallel pipelines, each pipeline being operable to transmit a subset of the units of data in a first-in-first-out manner, wherein the data units are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time, wherein the asynchronous circuit is operable to sequentially control transmission of the units of data in the pipelines such that the program order is maintained.

2. (Original) The circuit of claim 1 wherein the circuit comprises a processor and wherein the N-way-issue resource comprises an instruction pipeline.

3. (Original) The circuit of claim 1 wherein N comprises an integer greater than 1.

4. (Original) The circuit of claim 1 further comprising an M-way-issue resource, and interface circuitry operable to facilitate communication between the N-way-issue resource and the M-way-issue resource.

5. (Original) The circuit of claim 4 wherein M is fewer than N.

6. (Original) The circuit of claim 5 wherein M is 1 and N is 2.

7. (Original) The circuit of claim 4 wherein M is greater than N.

8. (Original) The circuit of claim 7 wherein M is 4 and N is 2.

9. (Original) The circuit of claim 4 wherein the interface circuitry is operable to facilitate transmission of selected ones of the data units from the N-way-issue resource to the M-way-issue resource.

10. (Original) The circuit of claim 4 wherein the interface circuitry is operable to facilitate transmission of selected ones of the data units from the M-way-issue resource to the N-way-issue resource.

11. (Original) The circuit of claim 4 wherein the interface circuitry is operable to facilitate transmission of first selected ones of the data units from the N-way-issue resource to the M-way-issue resource, and second selected ones of the data units from the M-way-issue resource to the N-way-issue resource.

12. (Original) The circuit of claim 11 wherein there is a one-to-one correspondence between the first and second selected data units.

13. (Original) The circuit of claim 11 wherein there is not a one-to-one correspondence between the first and second selected data units.

14. (Previously presented) The circuit of claim 4 wherein the asynchronous circuit comprises a processor and wherein each of the N-way-issue resource and the M-way-issue resource comprises one of an instruction dispatcher, a register file, an instruction cache, a branch predictor, an instruction fetch circuit, a writeback circuit, an instruction decoding circuit, an execution pipeline, and branch circuitry.

15. (Previously presented) The circuit of claim 4 wherein the interface circuitry is operable to identify selected ones of the data units in a higher order one of the resources for transmission to a lower order one of the resources.

16. (Previously presented) The circuit of claim 4 wherein the interface circuitry is operable to transmit selected ones of the data units generated by a lower

order issue one of the resources to a higher order issue one of the resources in such a way as to facilitate preservation of the program order.

17. (Original) The circuit of claim 1 wherein each pipeline is operable to transmit the units of data in accordance with an asynchronous handshake protocol.

18. (Original) The circuit of claim 17 wherein the asynchronous handshake protocol between a sender and a receiver in each of the pipelines comprises:

the sender sets a data signal valid when an enable signal from the receiver goes high;

the receiver lowers the enable signal upon receiving the valid data signal;

the sender sets the data signal neutral upon receiving the low enable signal; and

the receiver raises the enable signal upon receiving the neutral data signal.

19. (Original) The circuit of claim 18 wherein the handshake protocol is delay-insensitive.

20. (Original) The asynchronous circuit of claim 1 wherein each pipeline comprises a plurality of stages, corresponding stages in each pipeline being interconnected in a state loop operable to communicate state information among the pipeline stages.

21. (Previously presented) The circuit of claim 1 wherein the asynchronous circuit comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit.

22. (Previously presented) At least one computer-readable medium having data structures stored therein representative of an asynchronous circuit for processing units of data having a program order associated therewith, the asynchronous circuit being configured to employ asynchronous flow control to facilitate transmission of the data units, the asynchronous flow control being characterized by an average cycle time, the circuit comprising an N-way-issue

resource comprising N parallel pipelines, each pipeline being operable to transmit a subset of the units of data in a first-in-first-out manner, wherein the data units are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time, wherein the asynchronous circuit is operable to sequentially control transmission of the units of data in the pipelines such that the program order is maintained.

23-26. (Canceled)

27. (Previously presented) A set of semiconductor processing masks representative of an asynchronous circuit for processing units of data having a program order associated therewith, the asynchronous circuit being configured to employ asynchronous flow control to facilitate transmission of the data units, the asynchronous flow control being characterized by an average cycle time, the circuit comprising an N-way-issue resource comprising N parallel pipelines, each pipeline being operable to transmit a subset of the units of data in a first-in-first-out manner, wherein the data units are issued to the respective pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time, wherein the asynchronous circuit is operable to sequentially control transmission of the units of data in the pipelines such that the program order is maintained.

28. (Previously presented) A heterogeneous system for processing units of data having a program order associated therewith, the system comprising an N-way issue resource and at least one multiple-issue resource having an order different from N, the N-way issue resource being configured to employ asynchronous flow control to facilitate transmission of the data units, the asynchronous flow control being characterized by an average cycle time, the N-way issue resource being configured such that the units of data are issued to N parallel pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time, the system further comprising interface circuitry operable to facilitate communication between the N-way-issue resource and the at least one multiple-issue resource and to preserve the program order in all of the resources.

29. (Original) The system of claim 28 wherein the at least one multiple-issue resource comprises a plurality of multiple-issue resources having different orders.

30. (Original) The system of claim 28 wherein the interface circuitry comprises a dispatch circuit operable to route the data units received from the N-way issue resource on a first number of input channels to designated ones of a second number of output channels associated with the at least one multiple-issue resource in a deterministic manner thereby preserving a partial ordering for each output channel defined by the program order.

31. (Previously presented) The system of claim 28 wherein the N-way issue resource comprises first and second pipelines, and the interface circuitry comprises a dual filter comprising a dual-issue input datapath corresponding to the first and second pipelines, a single-issue output datapath, and a control channel, the dual filter being operable to selectively transmit data tokens on the input datapath to the output datapath according to control information on the control channel.

32. (Original) The system of claim 28 wherein the interface circuitry comprises remapping circuitry operable to route the data units received from the at least one multiple-issue resource on a first number of input channels to designated ones of a second number of output channels associated with the N-way issue resource in a manner which preserves the program order.

33. (Original) The system of claim 32 wherein the remapping circuitry comprises a crossbar circuit which is controlled by routing information generated when the data units are transmitted from the N-way issue resource to the at least one multiple-issue resource.

34. (Original) The system of claim 28 wherein the at least one multiple-issue resource comprises an M-way issue resource where M is an integer multiple of N, and wherein the interface circuitry comprises a plurality of split circuits which operate alternately to transmit the data units from the N-way issue resource to the M-

way issue resource, and a plurality of merge circuits which operate alternately to transmit the data units from the M-way issue resource to the N-way issue resource.

35. (Original) The system of claim 28 wherein the at least one multiple-issue resource comprises an M-way issue resource where M is less than N, and wherein the interface circuitry comprises at least one optional assign circuit which is operable to receive the data units from both of the N-way issue resource and M-way issue resource and to selectively transmit the received data units back into the N-way issue resource, thereby mitigating effects of a difference in throughput between the N-way issue resource and the M-way issue resource.

36. (Original) The system of claim 35 wherein the interface circuitry further comprises a crossbar circuit by which the data units are transmitted from the M-way issue resource to the at least one optional assign circuit.

37. (Original) The system of claim 35 wherein the at least one optional assign comprises first and second input datapaths, an output datapath, and a control input, the at least one optional assign being operable to transmit a first data token on the first input datapath to the output datapath when the control input is in a first state, the at least one optional assign further being operable to discard the first data token and to transmit a second data token on the second input datapath to the output datapath when the control input is in a second state.

38. (Original) The system of claim 37 wherein the at least one optional assign further being operable to discard the second data token and to transmit the first data token to the output datapath when the control input is in a third state.

39. (Original) The system of claim 28 wherein the interface circuitry comprises a dual repeat circuit comprising a single-issue data input channel, a dual-issue data output channel, and a control channel, the dual repeat circuit being operable in response to control information on the control channel to transmit a first data token on the input channel to the output channel and to maintain the first data token on the input channel for future use, the dual repeat circuit also being operable in response to the control information to transmit a second data token on the input

channel to the output channel and to discard the second data token so that the input channel can receive subsequent data token.

40. (Original) The system of claim 28 wherein the N-way issue resource has N pipelines associated therewith, and wherein the at least one multiple-issue resource has P pipelines associated therewith, and wherein N may be any of fewer than P, equal to P, or greater than P.

41. (Original) The system of claim 28 wherein there is a one-to-one correspondence between the data units in the N-way issue resource and the data units in the at least one multiple-issue resource.

42. (Original) The system of claim 28 wherein, at any given time, more of the data units are in the N-way issue resource than the at least one multiple-issue resource.

43. (Original) The system of claim 28 wherein the system comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit.

44. (Previously presented) At least one computer-readable medium having data structures stored therein representative of a heterogeneous system for processing units of data having a program order associated therewith, the system comprising an N-way issue resource and at least one multiple-issue resource having an order different from N, the N-way issue resource being configured to employ asynchronous flow control to facilitate transmission of the data units, the asynchronous flow control being characterized by an average cycle time, the N-way issue resource being configured such that the units of data are issued to N parallel pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time, the system further comprising interface circuitry operable to facilitate communication between the N-way-issue resource and the at least one multiple-issue resource and to preserve the program order in all of the resources.

45-48. (Canceled)

49. (Previously presented) A set of semiconductor processing masks representative of a heterogeneous system for processing units of data having a program order associated therewith, the system comprising an N-way issue resource and at least one multiple-issue resource having an order different from N, the N-way issue resource being configured to employ asynchronous flow control to facilitate transmission of the data units, the asynchronous flow control being characterized by an average cycle time, the N-way issue resource being configured such that the units of data are issued to N parallel pipelines staggered in time such that up to N data units enter the N pipelines during the average cycle time, the system further comprising interface circuitry operable to facilitate communication between the N-way-issue resource and the at least one multiple-issue resource and to preserve the program order in all of the resources.

10. EVIDENCE APPENDIX

[37 CFR 41.37(c)(1)(ix)]

No evidence has been submitted pursuant to §§ 1.130, 1.131, or 1.132 of 37 CFR, nor has any other evidence beyond the art of record been entered by the examiner.

11. RELATED PROCEEDINGS APPENDIX

[37 CFR 41.37(c)(1)(x)]

Included in this appendix is a copy of the Notice of Panel Decision from Pre-Appeal Brief Review dated July 16, 2008.